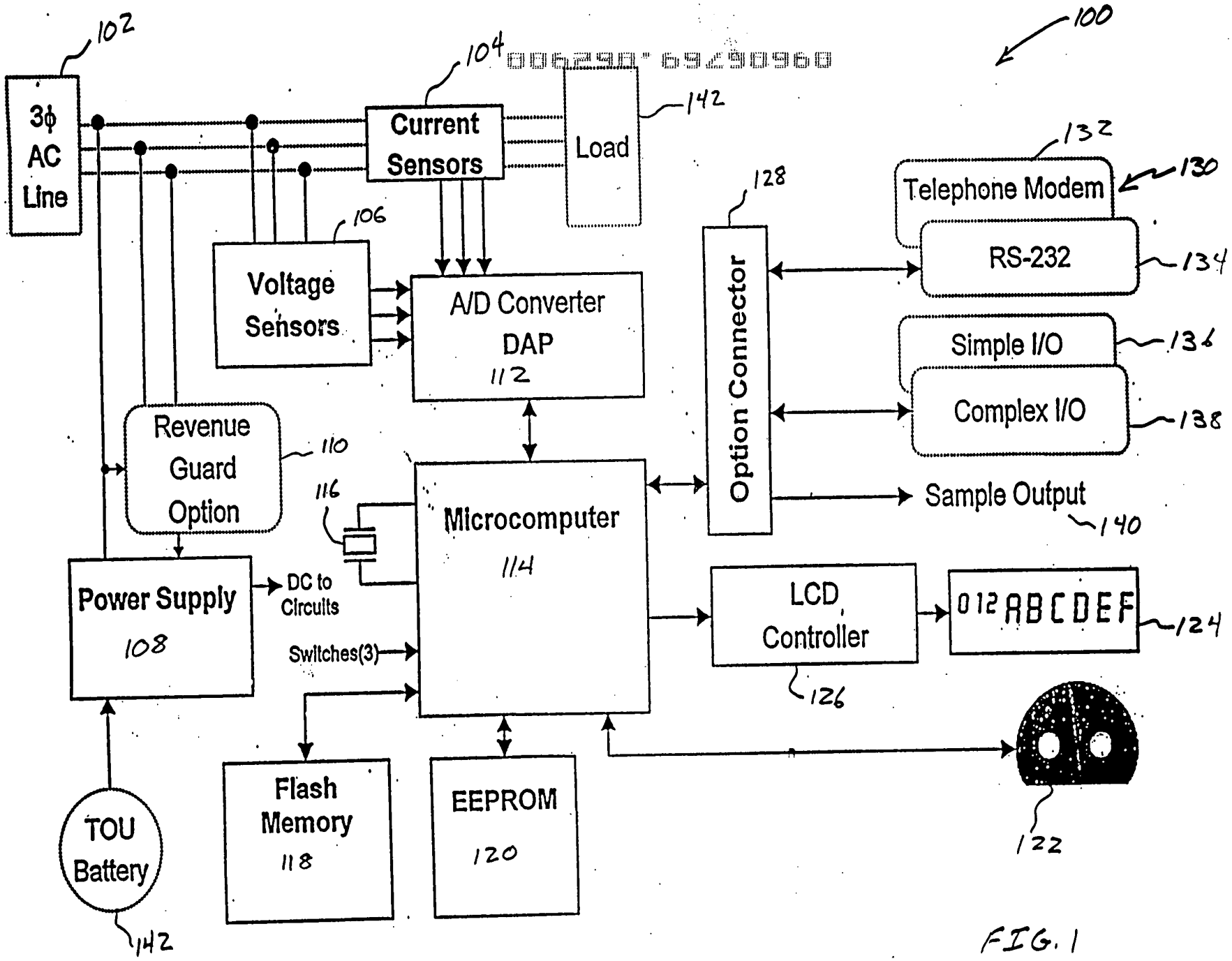
100
102
3φ AC Line
104
Current Sensors
Load
142
106
Voltage Sensors
A/D Converter DAP
112
128
Option Connector
132
Telephone Modem
130
RS-232
134
Simple I/O
136
Complex I/O
138
Sample Output
140
Revenue Guard Option
110
116
Microcomputer
114
Power Supply
108
DC to Circuits
Switches(3)
LCD Controller
126
012 ABCDEF
124
TOU Battery
142
Flash Memory
118
EEPROM
120
122

FIG. 1

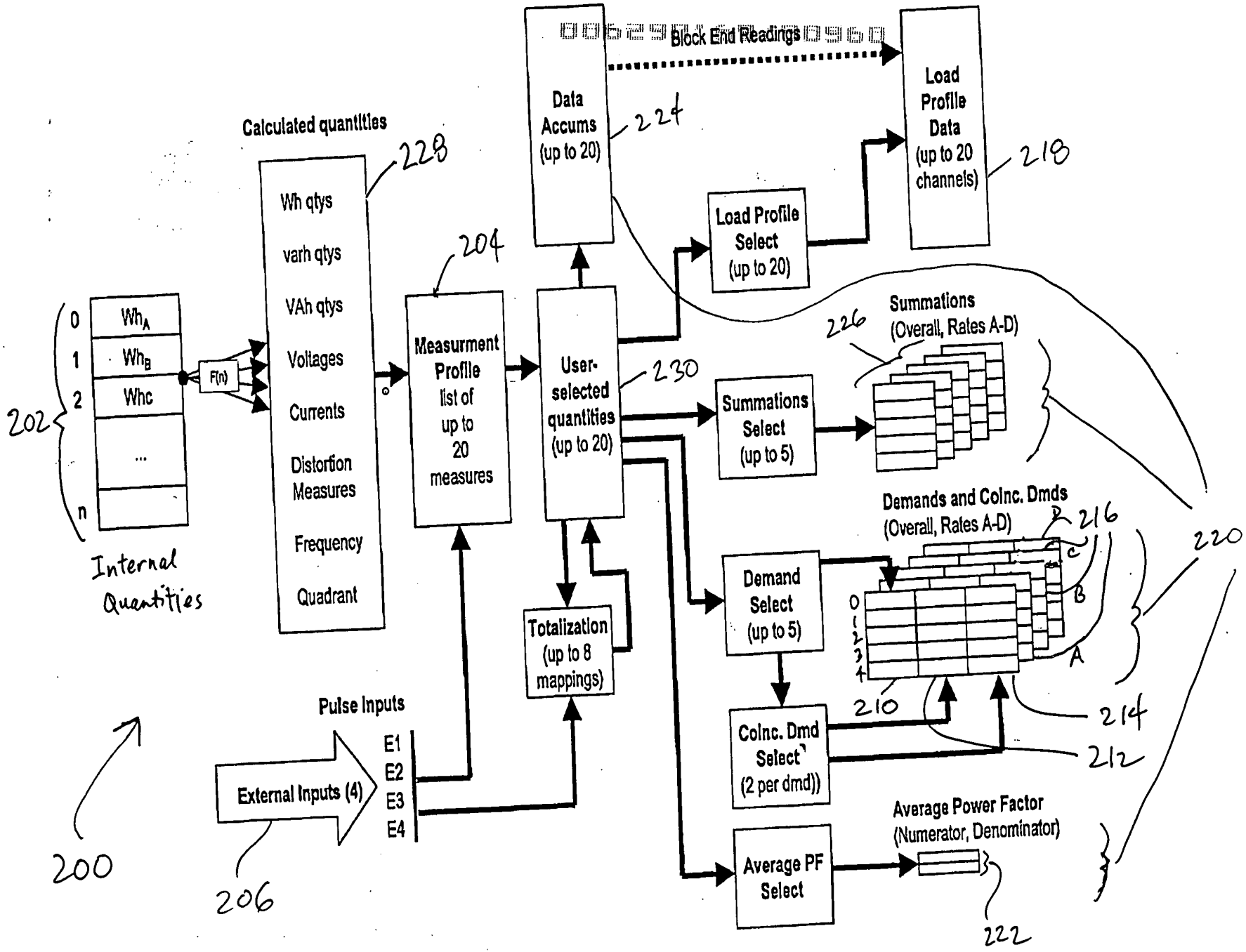
Block End Readings
Data Accums (up to 20)
224
Load Profile Data (up to 20 channels)
218
Load Profile Select (up to 20)
Calculated quantities
228
Wh qtys
varh qtys
VAh qtys
Voltages
Currents
Distortion Measures
Frequency
Quadrant
204
Measurment Profile list of up to 20 measures
User-selected quantities (up to 20)
230
Summations Select (up to 5)
226
Summations (Overall, Rates A-D)
Demands and Coinc. Dmds (Overall, Rates A-D)
216
220
Demand Select (up to 5)
Totalization (up to 8 mappings)
Coinc. Dmd Select (2 per dmd))
210
214
212
Pulse Inputs
E1
E2
E3
E4
External Inputs (4)
206
Average PF Select
Average Power Factor (Numerator, Denominator)
222
200
202
0
1
2
n
Wh_A
Wh_B
Whc
F(n)
Internal Quantities
A
B
C
D

Fig. 2

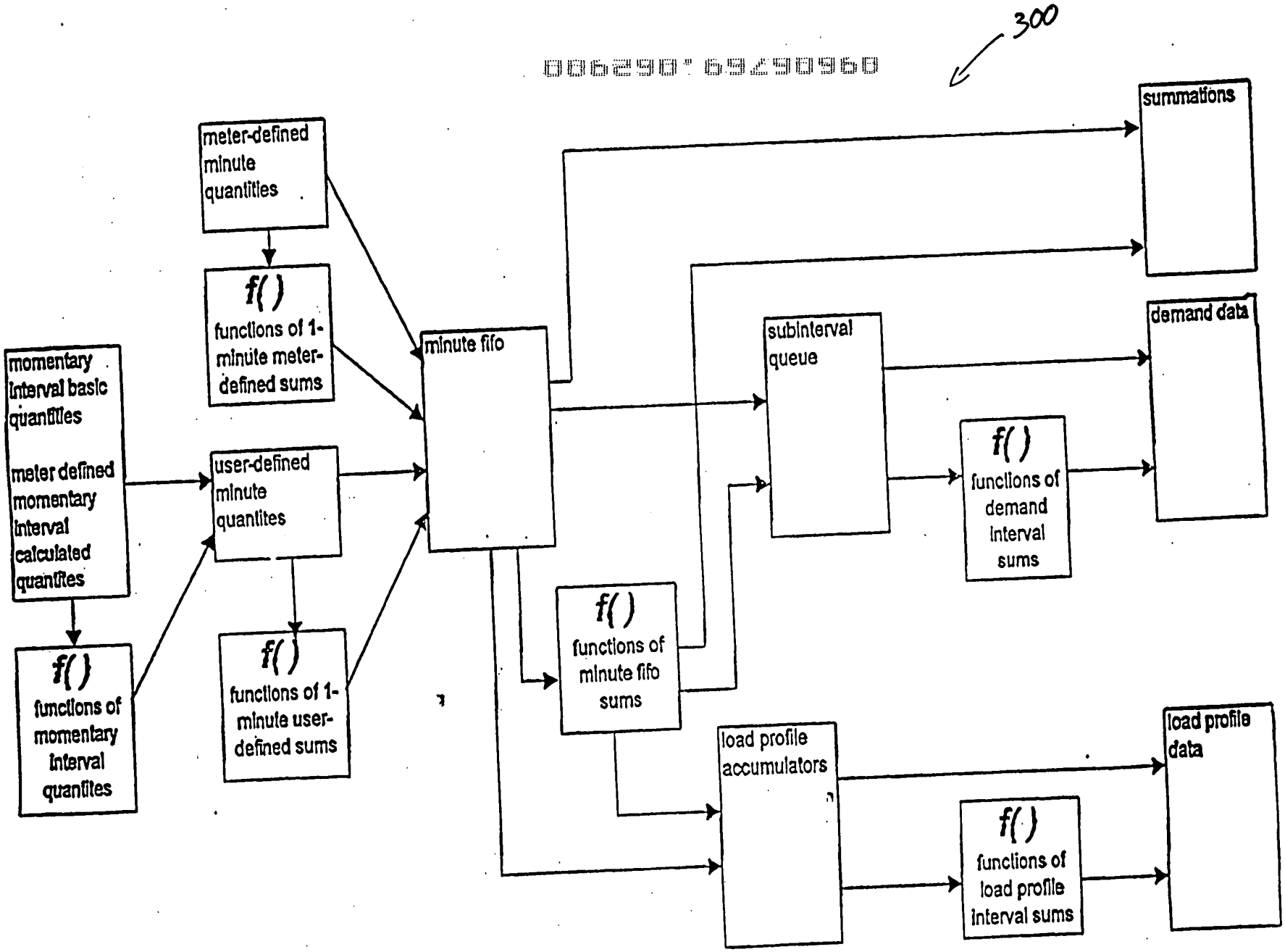

FIG.3

Signal	Normal Mode	ID Mode	Address Mode	Read Mode	Write Mode
I/O_LATCH	0	1	Hi-to-Lo Transition	0	0
I/O_READ	0	1	0	1	0
I/O_WRITE	0	0	0	0	Hi-to-Lo Transition
I/O_DATA_0	Hi-Z w/Pulldown	Address Bit 0	Address Bit 0	Input Bit 0	Output Bit 0
I/O_DATA_1	Hi-Z w/Pulldown	Address Bit 1	Address Bit 1	Input Bit 1	Output Bit 1
I/O_DATA_2	Hi-Z w/Pulldown	Address Bit 2	Address Bit 2	Input Bit 2	Output Bit 2
I/O_DATA_3	Hi-Z w/Pulldown	Response Bit 0	Sub-Address Bit 0	Input Bit 3	Output Bit 3
I/O_DATA_4	Hi-Z w/Pulldown	Response Bit 1	Sub-Address Bit 1	Lo-/Hi-Nibble	Lo-/Hi-Nibble

FIG. 4

Signal	ID Mode	Address Mode	Read Mode	Write Mode (Nib 0)
I/O_LATCH	1	Hi-to-Lo Transition	0	0
I/O_READ	1	0	1	0
I/O_WRITE	0	0	0	Hi-to-Lo Transition
I/O_DATA_0	1	0	N/A	KYZ 1 Output
I/O_DATA_1	0	0	N/A	KYZ 2 Output
I/O_DATA_2	0	0	N/A	Switch 1 Output
I/O_DATA_3	1	X	N/A	N/A
I/O_DATA_4	0	X	N/A	0

FIG. 5

Signal	ID Mode	Address Mode	Read Mode (Nib 0)	Read Mode (Nib 1)	Write Mode (Nib 0)	Write Mode (Nib 1)
I/O_LATCH	1	Hi-to-Lo Transition	0	0	0	0
I/O_READ	1	0	1	1	0	0
I/O_WRITE	0	0	0	0	Hi-to-Lo Transition	Hi-to-Lo Transition
I/O_DATA_0	1	1	Z1 Input	Z3 Input	KYZ1 Output	Switch 3 Output
I/O_DATA_1	0	0	Y1 Input	Y3 Input	KYZ2 Output	Switch 4 Output
I/O_DATA_2	0	0	Z2 Input	Z4 Input	Switch 1 Output	Switch 5 Output
I/O_DATA_3	0	X	Y2 Input	Y4 Input	Switch 2 Output	Switch 6 Output
I/O_DATA_4	1	X	0	1	0	1

FIG. 6